SHALLOW TRENCH POWER MOSFET AND IGBT

ABSTRACT OF THE DISCLOSURE

A power semiconductor device includes a substrate having an upper surface and a lower surface. The substrate has a trench. First and second doped regions are provided proximate the upper surface of the substrate. A first source region is provided within the first doped region. A second source region is provided within the second doped region. A gate is provided between the first and second source regions. The gate includes a first portion extending downward into the trench. A depth of the trench is no more than a depth of the first doped region.

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